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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,689	09/05/2003	Yian-Liang Kuo	TS03-337	6492
24504	7590	09/06/2005	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			NGUYEN, DILINH P	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/655,689	KUO ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 August 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 38-52 and 55-57 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 38-52 and 55-57 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>8/1/05</u>  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Claim Objections*

Claims 38 and 57 are objected to because of the following informalities:

Line 4, claim 38, replace "clip" with -- chip--.

Line 4, claim 57, replace "clip" with --chip--.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 38, 49-50 and 57 are rejected under 35 U.S.C. 102(b) as being anticipated by Shishido et al. (U.S. Pat. 6,294,831).

Shishido et al. disclose an ball grid array package, comprising:

a semiconductor chip/die 14 affixed to a ball grid substrate 12; the ball grid substrate having a series of balls 24; and

a heat spreader mounted to the semiconductor chip/die and the ball grid substrate opposite the series of balls; the heat spreader having a pattern of slots 48, not completely piercing the heat spreader, therein, wherein the pattern of the slots comprises a pattern selected from the group consisting of: circular pattern or a radiating pattern (cover fig., column 4, lines 40-50).

Art Unit: 2814

- Regarding claim 49, Shishido et al. disclose the slots penetrate the heat spreader from about 25 to 85 % (cover fig.).
- Regarding claim 50, Shishido et al. disclose that the slots penetrate the heat spreader from about 50 to 75% (cover fig.).
- Regarding claim 57, Shishido et al. disclose an ball grid array package, comprising:  
a semiconductor chip/die 14 affixed to a ball grid substrate 12, the ball grid substrate having a series of balls 24; and  
a heat spreader mounted to the semiconductor chip/die and the ball grid substrate opposite the series of balls; the heat spreader having a pattern of slots 48, not completely piercing the heat spreader, therein, wherein the slots penetrate the heat spreader from about 50 to 75% (cover fig., column 4, lines 40-50).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 39-40 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishido (U.S. Pat. 6294831) (newly cited) in view of Ho et al. (U.S. Pat. 2002/0079570) (previously applied).

Art Unit: 2814

- Regarding claims 39-40, Shishido substantially discloses all the limitations as claimed above except for the semiconductor chip is a silicon semiconductor chip.

However, Ho et al. disclose a silicon semiconductor chip (paragraph 0006, line 4). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replace the chip of Shishido et al. by a silicon semiconductor chip, as taught by Ho et al., such the silicon semiconductor chip is well known in the art for improving the heat dissipating characteristics (paragraph 0006).

- Regarding claims 45-46, Ho et al. disclose that the silicon semiconductor chip has a CTE approximately 3 ppm/°C and the heat spreader has a CTE of 18 ppm/°C (paragraph 0006).

5. Claims 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishido et al. (U.S. Pat. 6294831) (newly cited) in view of Kubo et al. (U.S. Pat. 6,199,273) (previously applied).

- Regarding claims 41-43, Shishido et al. substantially discloses all the limitations as claimed above. Shishido et al. also discloses that the heat spreader 18 is comprised of copper (fig. 1, column 3, lines 35-46).

Shishido et al. fail to disclose the balls are comprised of 63Sn37Pb, 96.5Sn3.5Ag, 5.5Sn3.8Ag0.7Cu or 96.2Sn2.5Ag0.8Cu0.5Sb.

However, Kubo et al. discloses that a solder ball is comprised of 63Sn37Pb (column 13, lines 36-37). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Shishido et al. by having the balls are comprised of 63Sn37Pb, as taught by Kubo et al, in order to

Art Unit: 2814

improve the electric contact characteristic for the semiconductor package (column 13, lines 36-40).

- Regarding claim 44, Kubo et al. disclose that the balls are comprised of 96.5Sn3.5Ag (column 14, lines 28-30).

6. Claims 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishido et al. (U.S. Pat. 6294831) (newly cited) in view of Ho et al. (U.S. Pat. 2002/0079570) (previously applied) and further in view of Jayaraman et al. (U.S. Pat. 6,724,091) (previously applied).

As discussed in details above the combination of Shishido and Ho et al. substantially disclose all the limitations as claimed above except for the chip is a germanium semiconductor chip and has a CTE of from about 5.5 to 6.5 or about 6.1.

However, Jayaraman et al. disclose that the semiconductor chip is a germanium semiconductor chip and has a CTE of about 6 ppm/° (column 1, lines 39-41).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to substitute the chip of the above combination by having a germanium semiconductor chip, as taught by Jayaraman et al., in order to use the semiconductor package in a particular application.

7. Claims 49-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishido et al. (U.S. Pat. 6562662) (newly cited) in view of Dordi (U.S. Pat. 5835355) (previously applied).

- Regarding claim 51, Shishido et al. do not explicitly disclose the pattern of slots include rows spaced apart from about 1.0 to 5.0 mm; the slots comprising each row are spaced apart from each other from about 0.5 to 2.5 mm.

However, Dordi (fig. 5) discloses a semiconductor package comprising a pattern of slots include rows spaced apart from about 1.0 to 5.0 mm (1.27mm or 5.08 mm, column 6, lines 10-15); the slots comprising each row are spaced apart from each other from about 0.5 to 2.5 mm (0.51mm or 1.27mm, fig. 4, column 6, lines 10-15).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of Shishido et al. by having the pattern of slots include rows spaced apart from about 1.0 to 5.0 mm; the slots comprising each row are spaced apart from each other from about 0.5 to 2.5 mm, as taught by Dordi, in order to reduce the amount of moisture from being trapped by the heat spreader and provide good heat dissipation for the semiconductor package (fig. 5, column 3, lines 27-29).

- Regarding claim 49, Dordi discloses that the slots penetrate the heat spreader from about 25 to 85% (fig. 4).
- Regarding claim 50, Dordi discloses that the slots penetrate the heat spreader from about 50 to 75% (fig. 4).
- Regarding claim 52, Dordi discloses that the pattern of slots includes rows spaced apart from about 1.5 to 2.5 mm (fig. 4, column 6, lines 10-15); the slots comprising each row are spaced apart from each other from about 0.7 to 1.5 mm (fig. 4, column 6, lines 10-15).

Art Unit: 2814

- Regarding claim 53, Dordi discloses that the pattern of slots 40 are arranged in: perpendicular/perpendicular rows; a square pattern (fig. 4).
- Regarding claim 54, Dordi discloses that the pattern of slots 40 are arranged in parallel/perpendicular rows (fig. 4).
- Regarding claims 55-56, Dordi discloses that the ball grid array package is a super ball grid array package (fig. 5).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

  
HOAI PHAM  
PRIMARY EXAMINER